WHAT IS CLAIMED IS:

METHOD OF FABRICATING A HIGH-LAYER-COUNT BACKPLANE

1. A method of fabricating a multi-layer circuit board, the method comprising:

creating a first layer arrangement comprising a plurality of high-speed differential trace layers and a plurality of reference plane layers stacked in an interleaved fashion, each high-speed differential trace layer separated from each adjacent reference plane layer by a layer of a first dielectric material;

creating a second layer arrangement comprising at least two patterned power plane layers, each having a thickness at least equivalent to the thickness of three-ounces-per-square-foot copper, stacked between layers of a second dielectric material having better void-filling capability, during lamination under similar conditions, than the first dielectric material;

laminating the first and second layer arrangements together such that the first and second layer arrangements interface across a reference plane layer; and

forming a large plurality of plated thru-holes distributed throughout the circuit board, the plated thru-holes electrically connecting the reference plane layers, while leaving the power plane layers electrically isolated from each other and from the reference plane layers, within the circuit board.

2. The method of claim 1, further comprising:

creating a third layer arrangement comprising a plurality of high-speed differential trace layers and a plurality of reference plane layers stacked in an interleaved fashion, each high-speed differential trace layer separated from each adjacent reference plane layer by a layer of the first dielectric material;

stacking the first, second, and third layer arrangements in that order; and

laminating the stacked layer arrangements together such that the second and third layer arrangements interface across a reference plane layer.

3. The method of claim 2, wherein after laminating, the second layer arrangement is substantially at the middle of the multi-layer circuit board.

4. The method of claim 2, wherein the at least two patterned power plane layers comprise four power plane layers, electrically isolated from each other and from the reference plane layers, within the circuit board.

5. The method of claim 4, further comprising forming a second plurality of plated thru-holes in the circuit board, the second plurality of plated thru-holes respectively connecting the four power plane layers to first power return, first power supply, second power supply, and second power return connector areas on the board surface.

6. The method of claim 4, wherein the step of creating a second layer arrangement comprises stacking the power plane layers with at least one low-speed trace layer and at least one reference plane layer separating that low-speed trace layer from the power plane layers, that low-speed trace layer and reference plane each stacked between layers of the second dielectric material.

7. The method of claim 1, wherein the first dielectric material comprises an allylated polyphenylene ether and the second dielectric material comprises an FR-4 resin.

8. The method of claim 1, wherein the first dielectric material has a lower dielectric loss than the second dielectric material at high-speed signaling frequencies.

9. The method of claim 8, wherein the first and second dielectric materials each comprise, prior to assembly, sheets of woven glass fiber impregnated with a filler, the second dielectric material having a higher percent-filler content than the first dielectric material.

10. The method of claim 9, wherein two sheets of the first dielectric material separate each high-speed differential trace layer from each adjacent reference plane layer.

11. The method of claim 1, wherein the high-speed differential trace layers each comprise a board region within a larger panel region, the panel region comprising a spaced-apart pattern of relatively small flow-impeding features near its periphery.

12. The method of claim 11, wherein the power plane layers comprise approximately the same board and panel regions as the high-speed differential trace layers, the panel region of each power plane layer comprising a substantially solid peripheral plane region having a relatively few patterned channels leading from the board region toward the edges of the panel.

13. A method of fabricating a multi-layer circuit board, the method comprising:

fabricating a plurality of high-speed core layers, each comprising a dielectric core of a first dielectric material with a patterned reference plane on one side and a plurality of patterned high-speed differential trace pairs on the opposite side;

fabricating at least one power core layer, comprising a dielectric core of a second dielectric material with a patterned power plane on at least one side, the patterned power plane having a thickness at least equivalent to the thickness of three-ounces-per-square-foot copper;

stacking the high-speed core layers and the at least one power core layer together with other layers, including b-stage dielectric layers of the first and second dielectric materials, the stacked layers arranged such that

at least two patterned power planes exist, separated by at least one layer of the second dielectric material,

each trace-pair side of a high-speed core layer abuts a b-stage layer of the first dielectric material,

each power-plane side of a power core layer abuts a b-stage layer of the second dielectric material,

a transition from the first dielectric material to the second dielectric material occurs across a reference plane, and

where two high-speed core layers are adjacent, the trace-pair side of one high-speed core layer faces the reference plane side of the other high-speed core layer;

laminating the stacked layers together; and

forming a large plurality of plated thru-holes distributed throughout the circuit board, the plated thru-holes electrically connecting the reference plane layers, the power plane layers remaining electrically isolated from each other and from the reference plane layers, within the circuit board.

14. The method of claim 13, further comprising forming each dielectric core using at least

two sheets of dielectric material.

15. The method of claim 13, wherein fabricating each high-speed core layer comprises forming, on the same side of the core as the high-speed differential trace pairs, a thieving pattern that maintains a minimum lateral separation from all high-speed differential traces on that layer, the minimum separation at least five times the spacing between the two traces of a high-speed differential trace pair.

16. The method of claim 13, further comprising treating the outward-facing conductive surfaces of each high-speed core layer to roughen those surfaces to approximately the same roughness as the roughness of the inward-facing conductive surfaces.

17. The method of claim 16, further comprising treating the outward-facing conductive surfaces of each power core layer to roughen those surfaces to a roughness greater than the roughness of the high-speed core layers.

18. A method of fabricating a multi-layer circuit board, the method comprising:

creating first and third layer arrangements, each comprising a plurality of high-speed differential trace layers and a plurality of reference plane layers stacked in an interleaved fashion, each high-speed differential trace layer separated from each adjacent reference plane layer by a layer of dielectric material;

creating a second layer arrangement comprising at least two patterned power plane layers, stacked between layers of a dielectric material;

laminating the first, second, and third layer arrangements together in that order, such that a reference plane layer on each side shields the second layer

arrangement from the high-speed differential trace layers; and

electrically connecting the reference plane layers to each other, while leaving the power plane layers electrically isolated from each other and from the reference plane layers, within the circuit board.

19. The method of claim 18, further comprising:

creating fourth and fifth layer arrangements, each comprising at least one low-speed trace layer;

laminating the fourth layer arrangement between the first and second layer arrangements, such that at least one reference plane separates the low-speed trace layer from the patterned power layers and at least one other reference plane separates the low-speed trace layer from the high-speed differential trace layers of the first layer arrangement; and

laminating the fifth layer arrangement between the second and third layer arrangements, such that at least one reference plane separates the low-speed trace layer from the patterned power layers and at least one other reference plane separates the low-speed trace layer from the high-speed differential trace layers of the third layer arrangement.

20. The method of claim 19, wherein the fourth layer arrangement comprises at least two low-speed trace layers separated by a dielectric layer, further comprising forming a thieving pattern on each of the two low-speed trace layers, and blending the thieving patterns such that the thieving pattern on one of the two trace layers does not overlay a trace on the other trace layer.

21. The method of claim 20, further comprising staggering the thieving patterns such that a thieving pattern feature on one of the two trace layers does not overlay a thieving pattern feature on the other trace layer.

22. The method of claim 21, wherein each thieving pattern comprises dots laid out on a square grid, the patterns staggered such that a dot feature on one trace layer generally overlays the center of a grid square on the other trace layer.

23. The method of claim 18, further comprising, during patterning of each patterned power layer, patterning a conductive guard ring adjacent the edges of the board and electrically direct-current isolated from the center conductive area of that power layer.

24. The method of claim 23, further comprising electrically connecting the guard rings to each other within the circuit board.